TEXAS INSTRUMENTS

TPS61130EVM

User's Guide

May 2003

PMP Portable Power

SLVU086

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third–party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Mailing Address:

Texas Instruments
Post Office Box 655303
Dallas, Texas 75265

EVM IMPORTANT NOTICE

Texas Instruments (TI) provides the enclosed product(s) under the following conditions:

This evaluation kit being sold by TI is intended for use for **ENGINEERING DEVELOPMENT OR EVALUATION PURPOSES ONLY** and is not considered by TI to be fit for commercial use. As such, the goods being provided may not be complete in terms of required design-, marketing-, and/or manufacturing-related protective considerations, including product safety measures typically found in the end product incorporating the goods. As a prototype, this product does not fall within the scope of the European Union directive on electromagnetic compatibility and therefore may not meet the technical requirements of the directive.

Should this evaluation kit not meet the specifications indicated in the EVM User's Guide, the kit may be returned within 30 days from the date of delivery for a full refund. THE FOREGOING WARRANTY IS THE EXCLUSIVE WARRANTY MADE BY SELLER TO BUYER AND IS IN LIEU OF ALL OTHER WARRANTIES, EXPRESSED, IMPLIED, OR STATUTORY, INCLUDING ANY WARRANTY OF MERCHANTABILITY OR FITNESS FOR ANY PARTICULAR PURPOSE.

The user assumes all responsibility and liability for proper and safe handling of the goods. Further, the user indemnifies TI from all claims arising from the handling or use of the goods. Please be aware that the products received may not be regulatory compliant or agency certified (FCC, UL, CE, etc.). Due to the open construction of the product, it is the user's responsibility to take any and all appropriate precautions with regard to electrostatic discharge.

EXCEPT TO THE EXTENT OF THE INDEMNITY SET FORTH ABOVE, NEITHER PARTY SHALL BE LIABLE TO THE OTHER FOR ANY INDIRECT, SPECIAL, INCIDENTAL, OR CONSEQUENTIAL DAMAGES.

TI currently deals with a variety of customers for products, and therefore our arrangement with the user **is not exclusive**.

TI assumes **no liability for applications assistance, customer product design, software performance, or infringement of patents or services described herein**.

Please read the EVM User's Guide and, specifically, the EVM Warnings and Restrictions notice in the EVM User's Guide prior to handling the product. This notice contains important safety information about temperatures and voltages. For further safety concerns, please contact the TI application engineer.

Persons handling the product must have electronics training and observe good laboratory practice standards.

No license is granted under any patent right or other intellectual property right of TI covering or relating to any machine, process, or combination in which such TI products or services might be or are used.

Mailing Address:

Texas Instruments
Post Office Box 655303
Dallas, Texas 75265

EVM WARNINGS AND RESTRICTIONS

It is important to operate this EVM within the input voltage range of 3.0 V to 5.5 V and the output voltage range of 2.5 V to 5.5 V for the SEPIC output and 0.9 V to 5.5 V for the LDO output.

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 85°C. The EVM is designed to operate properly with certain components above 60°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

Mailing Address:

Texas Instruments
Post Office Box 655303
Dallas, Texas 75265

Preface

Read This First

About This Manual

This user's guide describes the characteristics, operation, and use of the TPS61130EVM–206 SEPIC evaluation module (EVM). This EVM is a Texas Instruments high-efficiency, single Li-Ion input, dual output (SEPIC and LDO) converter that is configured to deliver 3.3 V at 300 mA and 1.5 V at 200 mA. The 3.3-V output is provided by the SEPIC converter and the 1.5-V output is provided by the integrated LDO. This user's guide includes setup instructions, a schematic diagram, a bill of materials (BOM), and PCB layout drawings for the evaluation module.

How to Use This Manual

This document contains the following chapters:

- Chapter 1—Introduction
- Chapter 2—Setup
- Chapter 3—Board Layout
- Chapter 4—Schematic and Bill of Materials

Related Documentation From Texas Instruments

TPS61130 data sheet (SLVS431)

If You Need Assistance. . .

Contact your local TI sales representative.

FCC Warning

This equipment is intended for use in a laboratory test environment only. It generates, uses, and can radiate radio frequency energy and has not been tested for compliance with the limits of computing devices pursuant to subpart J of part 15 of FCC rules, which are designed to provide reasonable protection against radio frequency interference. Operation of this equipment in other environments may cause interference with radio communications, in which case the user at his own expense will be required to take whatever measures may be required to correct this interference.

Contents

Figures

Tables

Chapter 1

Introduction

The Texas Instruments TPS61130EVM evaluation module (EVM) helps designers evaluate the operation and performance of the TPS61130 family of devices. These devices are high efficiency SEPIC converters that offer an integrated LDO.

This EVM is specifically designed and optimized to operate from a Li-Ion input (3.0 V to 4.2 V). Operation at input voltages less than 3.0 V is possible with reduced output current. The default output voltages of this EVM are 3.3 V for the SEPIC output and 1.5 V for the LDO output. If desired, this EVM can easily be modified to supply higher or lower output voltages. The SEPIC converter can be set up to provide an output voltage between 2.5 V and 5.5 V. The LDO can be set up to provide an output voltage between 0.9 V and 5.5 V. Output voltages other than the default values may be evaluated by adjusting the appropriate feedback resistor dividers. Also, other fixed output voltage versions of the devices can be easily evaluated using this EVM. Refer to the data sheet (SLVS431) for the various fixed output voltage options available in the TPS6113x device family as well as for more information on adjusting the output voltage.

Chapter 2

Setup

This chapter describes the jumpers and connectors on the EVM as well as how to properly connect, setup, and use the TPS61130EVM–206.

Topic **Page**

2.1 Input/Output Connector Descriptions

2.1.1 J1 – VBAT

This is the positive connection to the input power supply. The leads to the input supply should be twisted and kept as short as possible to minimize EMI transmission.

2.1.2 J2 – GND

This is the return connection for the input power supply.

2.1.3 J3 – VOUT

This is the positive connection from the output of the SEPIC power supply. Connect this pin to the positive input of the load.

2.1.4 J4 – GND

This is the negative connection from the output of the SEPIC power supply. Connect this pin to the negative input of the load.

2.1.5 J5 – LDOOUT

This is the positive connection from the output of the LDO power supply. Connect this pin to the positive input of the load.

2.1.6 J6 – GND

This is the negative connection from the output of the LDO power supply. Connect this pin to the negative input of the load.

2.1.7 J7 – PGOOD, LBO

Pin 1 of this jumper is the PGOOD output of the TPS61130. Pin 2 of this jumper is the LBO output of the TPS61130. Both signals are pulled up to Vout through a 1-MΩ resistor on the PCB.

2.1.8 JP1 – SKIPEN

This jumper enables or disables SKIPEN by connecting the shorting jumper to either the ON or OFF position. With SKIPEN set ON the part goes into a more efficient pulse skip mode of operation at light loads.

2.1.9 JP2 – EN

This jumper enables and disables the SEPIC portion of the EVM.

2.1.10 JP3 – LDOEN

This jumper enables and disables the LDO portion of the EVM.

2.1.11 JP4 – LDOIN

This is the input connection to the integrated LDO of the TPS61130. Shorting the VBAT pin and the center pin connects the VBAT input of the EVM to the LDOIN on the TPS61130. Shorting the VOUT pin and the center pin connects the VOUT pin of the EVM to the LDOIN on the TPS61130. This jumper may be removed and any voltage up to 5.5 V can be applied to the input of the LDO by directly connecting a voltage source to the center pin of JP4.

2.2 Setup

Connect an input supply between J1 and J2. The voltage range on this supply should stay between 3.0 V and 5.5 V. Connect a load for the SEPIC converter between J3 and J4. Connect a load for the LDO between J5 and J6. Configure the SKIPEN jumper to the desired setting. Configure JP4 to provide power to the LDO from the desired source.

2.3 Operation

The EVM has been optimized to operate from a Li-Ion battery input voltage range (3.0 V to 4.2 V). The SEPIC output voltage is set to 3.3 V and is capable of supplying 300 mA. The LDO output is set to 1.5 V and is capable of supplying 200 mA. After connecting the input and output connections, and setting the SKIPEN jumper (JP1) to the desired setting, turn on the input supply, and then enable the outputs as desired with JP2 and JP3.

The resistor divider on the LBI pin is designed to trip the LBO output when the input supply voltage drops below 2.9 V.

Chapter 3

Board Layout

This chapter provides the TPS61130EVM–206 board layout and illustrations.

Topic **Page**

3.1 Layout

Board layout is critical for all switch mode power supplies. Figures 1, 2, and 3 show the board layout for the TPS61130EVM–206 PWB. The nodes with high switching frequencies and currents are short and are isolated from the noise sensitive feedback circuitry. Careful attention has been given to the routing of high frequency current loops. Refer to the data sheet for specific layout guidelines.

Figure 3–1. Top Layer

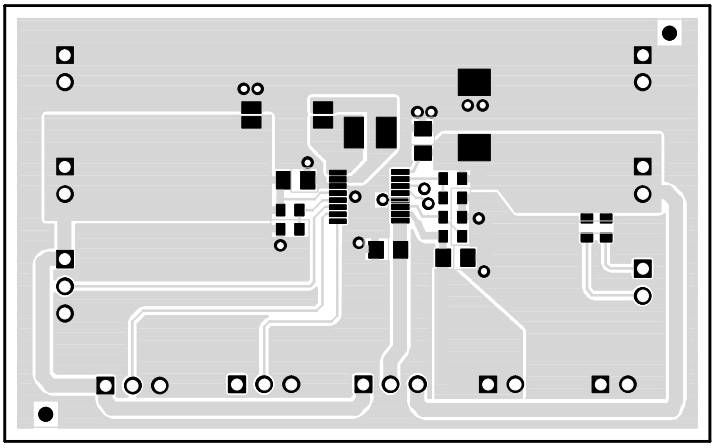


Figure 3–2. Bottom Layer

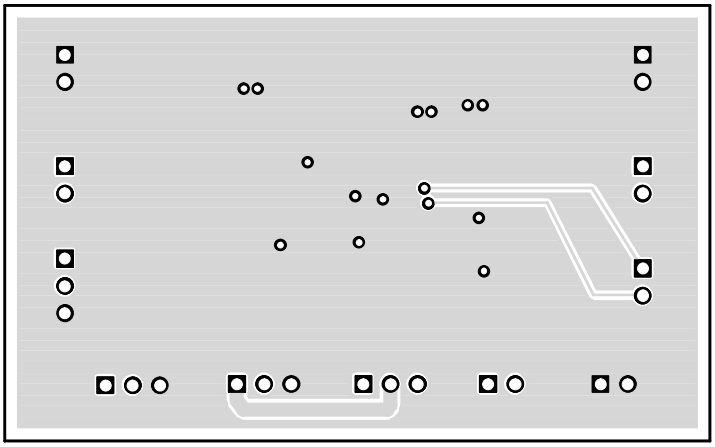
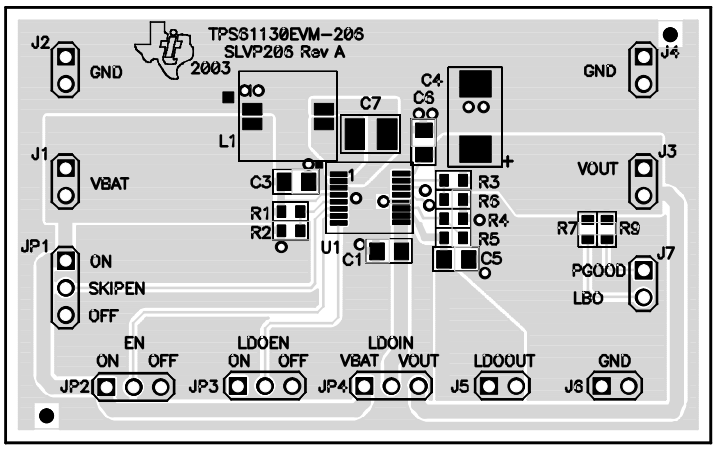


Figure 3–3. Top Assembly



Chapter 4

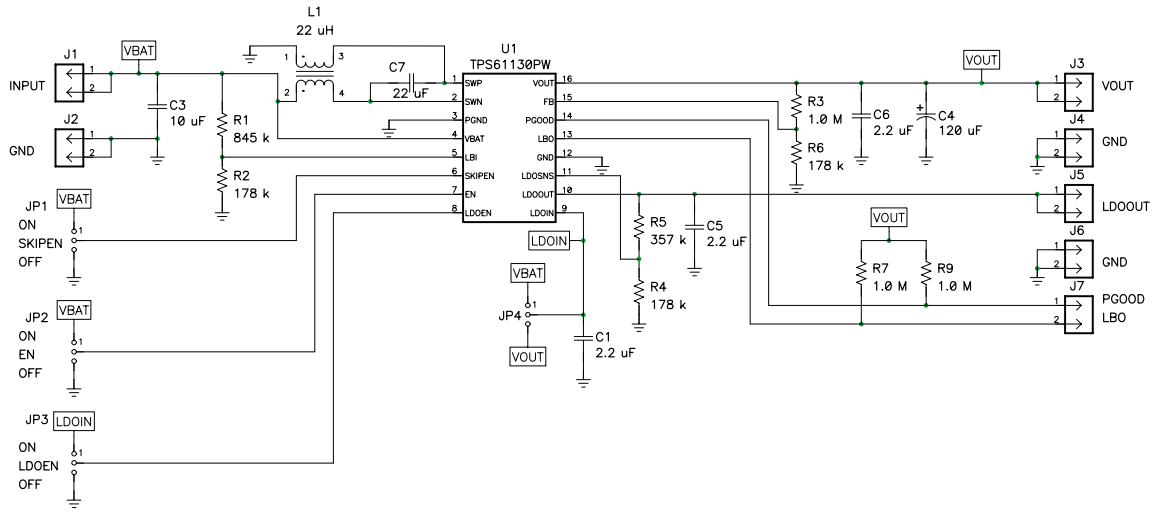
Schematic and Bill of Materials

This chapter provides the TPS61130EVM–206 schematic and bill of materials.

Topic **Page**

4.1 Schematic

Figure 4–1. TPS61130EVM–206 Schematic



4.2 Bill of Materials

Table 4–1. TPS61130EVM–206 Bill of Materials

COUNT	Ref Des	DESCRIPTION	SIZE	MFR	PART NUMBER
3	C1, C5, C6	Capacitor, ceramic, 2.2-µF, 6.3-V, X5R, 10%	805	Murata	GRM21BR60J225KC01B
1	C3	Capacitor, ceramic, 10-µF, 6.3-V, X5R, 10%	805	Murata	GRM21BR60J106KE01
1	C4	Capacitor, tantalum, 120-µF, 10-V, 140-mΩ, 20%	7343 (D)	Vishay	595D127X0010D2T
1	C7	Capacitor, ceramic, 22-µF, 10-V, X5R, 10%	1210	Murata	GRM32ER61A226KA65
7	J1– J7	Header, 2-pin, 100-mil spacing, (36-pin strip)	0.100 In x 2 In	Sullins	PTC36SAAN
4	JP1–JP4	Header, 3-pin, 100-mil spacing, (36-pin strip)	0.100 In x 3 In	Sullins	PTC36SAAN
1	L1	Inductor, SMT, 22-µH, 811-mA, 429-mΩ	0.300 In x 0.300 In	Coiltronics	DRQ74–220
1	R1	Resistor, chip, 845-kΩ, 1/16-W, 1%	603	Std	Std
3	R2, R4, R6	Resistor, chip, 178-kΩ, 1/16-W, 1%	603	Std	Std
3	R3, R7, R9	Resistor, chip, 1-MΩ, 1/16-W, 1%	603	Std	Std
1	R5	Resistor, chip, 357-kΩ, 1/16-W, 1%	603	Std	Std
1	U1	IC, single cell or dual cell Li-Ion boost/sepic converter	TSSOP-16	TI	TPS61130PW
1	—	PCB, 2.6 In x 1.6 In x 0.062 In		Any	SLVP206
4	—	Shunt, 100-mil, black	0.100 In	3M	929950–00